What is claimed is:

1. A semiconductor integrated circuit including a memory which can enter active state or standby state,

wherein said memory has voltage generation circuits for bit lines and source lines with which memory cells are connected, and

wherein said voltage generation circuits make the potential of said bit lines and the potential of said source lines equal to each other in response to an instruction to transition from said active state to said standby state, and produce a potential difference between said bit lines and said source lines in response to an instruction to transition from said standby state to said active state.

2. The semiconductor integrated circuit according to Claim 1,

wherein said voltage generation circuits make the potential of said source lines equal to the precharge potential of said bit lines in response to an instruction to transition from said active state to said standby state.

3. The semiconductor integrated circuit according to Claim 1,

wherein said voltage generation circuits make the potential of said bit lines equal to the discharge potential of said source lines in response to an instruction to transition

from said active state to said standby state.

4. The semiconductor integrated circuit according to Claim 2,

wherein said voltage generation circuits discharge the source lines in response to an instruction to transition from said standby state to said active state, and the current supplying capability thereof is varied so that the discharge rate will be enhanced stepwise.

5. A semiconductor integrated circuit which comprises: a central processing unit; and a memory accessible from said central processing unit, and can enter active state or standby state,

wherein said memory includes memory cells connected with bit lines and source lines, and makes the potential of said bit lines and the potential of said source lines equal to each other in said standby state and can produce a potential difference between said bit lines and said source lines in said active state.

6. The semiconductor integrated circuit according to Claim 5,

wherein in said standby state, said central processing unit stops instruction execution, and the memory stops access operation.

7. The semiconductor integrated circuit according to Claim 6,

wherein instructions to transition from said active state to said standby state and instructions to transition from said standby state to said active state are given by an external control signal.

8. The semiconductor integrated circuit according to Claim 6,

wherein instructions to transition from said active state to said standby state are given by the central processing unit executing a predetermined instruction, and instructions to transitions from said standby state to said active state are given by an interrupt.

9. A semiconductor integrated circuit including: a memory which can enter active state or standby state; and a central processing unit which can access said memory,

wherein said memory has memory cells connected with bit lines and source lines, and makes the potential of said source lines equal to the precharge potential of said bit lines in said standby state and brings the source lines to discharge potential in said active state.

10. A semiconductor integrated circuit including: a memory

which can enter active state or standby state; and a central processing unit which can access said memory,

wherein said memory has memory cells connected with bit lines and source lines, and makes the potential of said bit lines equal to the discharge potential of said source lines in said standby state and brings the bit lines to precharge potential in said active state.

11. The semiconductor integrated circuit according to Claim 9,

wherein the central processing unit is brought into a state in which instruction execution is stopped in parallel with said memory entering standby state, and said standby state and said state in which instruction execution is stopped can be released by an interrupt or external control signal.

12. A semiconductor integrated circuit including: a central processing unit; and a memory accessible from said central processing unit,

wherein said memory has bit lines connected with a first circuit, source lines connected with a second circuit, and memory cells which are connected with said bit lines and said source lines and whose select terminals are connected with word lines,

wherein said semiconductor integrated circuit can select first state in which the access operation of said memory and the data processing operation of the central processing unit

are enabled, and second state in which the access operation of said memory and the data processing operation of the central processing unit are disabled, and

wherein in said first state, said first circuit charges the bit lines and said second circuit discharges the source lines, and in said second state, said first circuit charges the bit lines and said second circuit charges the source lines.

13. A semiconductor integrated circuit including: a central processing unit; and a memory accessible from said central processing unit,

wherein said memory has bit lines connected with a first circuit, source lines connected with a second circuit, and memory cells which are connected with said bit lines and said source lines and whose select terminals are connected with word lines,

wherein said semiconductor integrated circuit can select first state in which the access operation of said memory and the data processing operation of the central processing unit are enabled, and second state in which the access operation of said memory and the data processing operation of the central processing unit are disabled, and

wherein in said first state, said first circuit charges the bit lines and said second circuit discharges the source lines, and in said second state, said first circuit discharges the bit lines and said second circuit discharges the source line.

14. The semiconductor integrated circuit according to Claim 13,

wherein the ultimate level of said discharge is equal to the ground potential of the circuit and the unselect level of said word lines is equal to the ground potential of the circuit.

15. The semiconductor integrated circuit according to Claim 13,

wherein in said first state, said first circuit stops the operation of charging the bit lines through which readout is carried out.

16. An IC card mounted with a semiconductor integrated circuit and an external interface portion connected with said semiconductor integrated circuit over a card substrate,

wherein said semiconductor integrated circuit includes a central processing unit and a memory accessible from said central processing unit, and

wherein said memory has memory cells connected with bit lines and source lines and makes the potential of said bit lines and the potential of said source lines equal to each other when said semiconductor integrated circuit is in low-power consumption state.

17. The IC card according to Claim 16,

wherein said memory is a mask ROM.

18. An IC card including, over a card substrate, a semiconductor integrated circuit and external connection electrodes,

wherein said semiconductor integrated circuit is selectively brought into standby state or active state, and has a central processing unit and a memory, and

wherein said memory has memory cells connected with bit lines and source lines, and in said active state, a predetermined potential difference is produced between said bit lines and said source lines and in said standby state, the potential difference between said bit lines and said source lines is reduced to a value smaller than the potential difference in said active state.

19. The IC card according to Claim 18,

wherein said central processing unit executes a sleep instruction in active state, and transitions to said standby state.

20. The IC card according to Claim 19, including a clock pulse generator which generates internal clock from external clock,

wherein the clock pulse generator outputs internal clock in active state and stops the output of internal clock in standby

state.

21. The IC card according to Claim 20, including a regulator which generates internal supply voltage from external supply voltage,

wherein in standby state, the regulator lowers internal supply voltage to a value lower than the internal supply voltage in active state.

22. An IC card having on a card substrate a semiconductor integrated circuit and external connection electrodes,

wherein said semiconductor integrated circuit is selectively brought into standby state or active state, and has a central processing unit and a memory,

wherein said memory has memory cells connected with bit lines and source lines,

wherein said semiconductor integrated circuit carries out initialization in response to a reset instruction from the outside,

wherein said semiconductor integrated circuit notifies the outside of the completion of the initialization to transition to active state,

wherein in active state, said semiconductor integrated circuit produces a predetermined potential difference between said bit lines and said source lines of the memory and causes the central processing unit to process data in response to an

instruction from the outside,

wherein said semiconductor integrated circuit transitions to standby state by the central processing unit executing a sleep instruction,

wherein in standby state, said semiconductor integrated circuit reduces the potential difference between said bit lines and said source lines of said memory to a value smaller than the potential difference in active state, and

wherein said semiconductor integrated circuit transitions to active state in response to a standby release signal, and in the process of the transition, produces a predetermined potential difference between said bit lines and said source lines by source line discharge and enhances the discharge rate stepwise.

23. A semiconductor integrated circuit which includes: memory cells connected with bit lines and source lines; and voltage generation circuits for the bit lines and the source lines, and is selectively brought into standby state or active state,

wherein in said active state, said voltage generation circuits produce a predetermined potential difference between said bit lines and said source lines, and in said standby state, said voltage generation circuits reduce the potential difference between said bit lines and said source lines of said memory to a value smaller than the potential difference in active

state.

24. The semiconductor integrated circuit according to Claim 23,

wherein in the process of the semiconductor integrated circuit transitioning from standby state to active state, said voltage generation circuits produce said predetermined potential difference between said bit lines and said source lines by source line discharge, and enhance the discharge rate stepwise.